CLAIMS

What is claimed is:

1. A capacitor within a substrate assembly, comprising:

a first electrode having a container shape defining a planar top surface;

a dielectric over said first electrode; and

a second electrode over said dielectric and extending from said container shape at at least two different levels within said substrate assembly.

2. The capacitor in claim 1, wherein said second electrode extends from said container shape at a first level and at a second level, and wherein said first level and said second level define a difference in height of at least 500 angstroms.

3. The capacitor in claim 2, wherein said first level and said second level define a difference in height of at least 1000 angstroms.

4. The capacitor in claim 3, wherein said first level and said second level define a difference in height of at least 2000 angstroms.

5. The capacitor in claim 1, wherein said second electrode comprises:

a first portion extending from said container shape at a first level lower than a top of said container shape; and

a second portion extending from said container shape at a second level higher than said first level.

6. The capacitor in claim 1, wherein said second electrode comprises:

a first portion extending from said container shape at a first level at least as high as a top of said container shape; and

a second portion extending from said container shape at a second level lower than said first level.

7. The capacitor in claim 6, wherein said dielectric extends from said container shape under said first and second portion of said second electrode.

8. A storage device environment, comprising:

a first plate defining a uniform vertical length;

at least one material external to said first plate;

a capacitor dielectric contacting said first plate, wherein:

said first plate, a first portion of said at least one material, and said capacitor dielectric meet at a first elevation along said vertical length; and

said first plate, a second portion of said at least one material, and said capacitor dielectric meet at a second elevation along said vertical length; and

a second plate contacting said capacitor dielectric.

9. The storage device environment in claim 8, wherein said second plate and said

capacitor dielectric are coextensive.

10. The storage device environment in claim 8, wherein said first portion of said at least one material is from a first material; and wherein said second portion of said at least one material is a from a second material.

11. The storage device environment in claim 10, wherein said first material and said second material are dielectric.

12. The storage device environment in claim 11, wherein said first portion of said at least one material encompasses a contact site.

13. An array of capacitors, comprising:

a first bottom capacitor plate;

a second bottom capacitor plate;

a third bottom capacitor plate;

a contact between said first bottom capacitor plate and said second bottom capacitor plate;

a trench between said second bottom capacitor plate and said third bottom capacitor plate;

a common top capacitor plate over said first bottom capacitor plate, said second bottom capacitor plate, and said third bottom capacitor plate, wherein said top capacitor plate extends toward said contact at a first level within said

array and is separate from said contact, and wherein said top capacitor plate lines a side of said trench and further lines a bottom of said trench at a second level within said array; and

a dielectric between said top capacitor plate and said first, second, and third bottom capacitor plates.

14. The array in claim 13, wherein said top capacitor plate extends toward a top of said contact.

15. A container capacitor structure, comprising:

a cup-shaped electrode having an interior surface and an exterior surface, wherein said exterior surface comprises a first portion and a second portion coextensive in height with said first portion;

an insulating layer contacting the exterior surface on the first portion;

a dielectric layer disposed on the interior surface and on the exterior surface on said second portion; and

a conductor layer disposed on the dielectric layer.

16. The container capacitor structure of claim 15, wherein the cup-shaped electrode comprises hemispherical-grain-silicon.

17. The container capacitor structure of claim 15, wherein the cup-shaped electrode has an interior width of no greater than 200 nm.

18. The container capacitor structure of claim 15, wherein the cup-shaped electrode has an exterior width of no greater than 300 nm.

19. A portion of a memory array having memory cells operatively coupled to row lines and column lines, the portion of the memory array comprising:

a plurality of contacts;

a plurality of container capacitors proximal to the contacts, each of the container capacitors having a bottom electrode, a dielectric, and a top electrode; wherein each bottom electrode has a cup-shape; wherein the dielectric is disposed on and in each container capacitor and further disposed between at least one pair of bottom electrodes of the plurality of container capacitors; and wherein the top electrode is disposed on the dielectric, in each container capacitor, and between the at least one pair of bottom electrodes; and

an insulating layer disposed between the contacts and bottom electrodes.

20. The portion of the memory array of claim 19, wherein the column lines are on a pitch of no greater than 0.5 microns.

21. The portion of the memory array of claim 20, wherein each of the contacts is surrounded by six of the container capacitors.

22. The portion of the memory array of claim 21, wherein each of the contacts has a critical dimension of no greater than 0.32 microns.

23. In a dynamic random access memory array, at least a portion of the memory array comprising:

a plurality of bit lines;

a plurality of contacts operatively coupled to the bit lines;

a plurality of memory cells operatively coupled to the contacts, each of the memory cells having a container capacitor, the memory cells arranged such that container capacitors are disposed around a contact;

container capacitor bottom electrodes spaced apart from one another and spaced apart from the contact;

container capacitor dielectric disposed between the container capacitor bottom electrodes and not disposed between the contact and the container capacitor bottom electrodes; and

a container capacitor top electrode disposed between the container capacitor bottom electrodes and not disposed between the contact and the container capacitor bottom electrodes.

24. The portion of the memory array of claim 23, wherein the bit lines are disposed above the container capacitors.

25. The portion of the memory array of claim 24, wherein the bit lines are on a pitch of no greater than 0.5 microns.

26. Container capacitor structures, comprising:

bottom electrodes having a cup-shape, the bottom electrodes having an interior surface and an exterior surface;

at least one insulating layer in contact with the exterior surface of the cup-shaped bottom electrodes and defining a recess between a first pair of cup-shaped bottom electrodes;

a dielectric layer disposed on the interior surface of the cup-shaped bottom electrodes and on the exterior surface between the first pair of the cup-shaped bottom electrodes; and

a top electrode layer on the dielectric layer opposite the interior surface of the cup-shaped bottom electrodes and opposite the exterior surface between the first pair of the cup-shaped bottom electrodes.

27. The container capacitor structures in claim 26, wherein said at least one insulating layer defines a contact site between a second pair of the cup-shaped bottom electrodes.

28. The container capacitor structures in claim 26, wherein the first pair of the cup-shaped bottom electrodes and the second pair of the cup-shaped bottom electrodes share a common cup-shaped bottom electrode.

29. A method for forming a container capacitor, comprising the steps of:

providing a cup-shaped bottom electrode;

providing an insulating layer around an exterior surface of said cup-shaped bottom

electrode;

masking a first portion of said insulating layer;

etching a second portion of said insulating layer from a part of said exterior surface;

depositing a dielectric layer on said part of said exterior surface; and

depositing a conductive layer on said dielectric layer.

30. A method for forming at least a portion of a memory array, comprising the steps of:

providing a substrate assembly;

providing a plurality of cup-shaped electrodes on said substrate assembly;

providing an insulating layer around exterior surfaces of said cup-shaped electrodes;

masking a portion of said insulating layer;

etching recesses into said insulating layer in unmasked regions between the cup-shaped electrodes, said etching exposing portions of said exterior surfaces;

depositing a dielectric layer on exposed portions of said exterior surfaces; and

depositing a conductive layer on said dielectric layer.

31. A method for forming a portion of a memory array, comprising the steps of:

providing a substrate assembly;

providing an insulating layer on said substrate assembly, said insulating layer having holes formed therein;

providing a container capacitor bottom electrode in each of said holes of said insulating layer;

masking a portion of said insulating layer and leaving mask gaps between adjacent container capacitor bottom electrodes;

forming recesses in said insulating layer according to said mask gaps;

depositing a dielectric into said recesses; and

depositing a conductor on said dielectric and into said recesses.

32. A method for forming a portion of a memory array, comprising the steps of:

providing a substrate assembly;

providing an insulating layer on said substrate assembly;

forming holes in said insulating layer;

forming a cup-shaped electrode in each of said holes;

covering a portion of said insulating layer with a mask layer; and

etching recesses in unmasked portions of said insulating layer between adjacent cup-shaped electrodes.

33. A substrate assembly, comprising:

a plug;

a first dielectric surrounding said plug; and

a vertical capacitor structure comprising:

a first electrode having:

a first outer area facing said plug and contacting said first dielectric,

and

a second outer area facing away from said plug,

a second electrode conformal to said second outer area and excluded from a region between said plug and said first outer area, and

a second dielectric between said first electrode and said second electrode.

34. The substrate assembly in claim 33, wherein said vertical capacitor structure is a stud capacitor.

35. A method of preparing a DRAM, comprising:

providing a first dielectric layer;

designating a plurality of contact sites within said first dielectric layer;

forming a plurality of first vertical capacitor electrodes in said first dielectric layer and among said plurality of contact sites; and

defining a plurality of discrete portions of said first dielectric layer, wherein each discrete portion extends from a contact site to first vertical capacitor electrodes around said contact site.

36. The method in claim 35, further comprising:

providing a second dielectric layer over said plurality of first vertical capacitor electrodes, over said plurality of discrete portions of said first dielectric layer, and between said plurality of discrete portions of said first dielectric layer;

providing a second vertical capacitor electrode over said second dielectric layer; and

removing said second dielectric layer and said second vertical capacitor electrode from areas extending over said plurality of contact sites and beyond.

37. A method of configuring a container capacitor including a bottom electrode, comprising:

allowing for capacitance using a first portion of an exterior surface of said bottom electrode, wherein said first portion is askew from a contact; and

allowing for capacitance without using a second portion of said exterior surface, wherein said second portion faces said contact.

38. A circuit, comprising:

a first circuit device defining an axis; and

a second circuit device comprising:

a far side distal from said first circuit device,

a near side proximate said first circuit device, and

an element defining:

a plurality of layers at said far side, wherein each layer of said plurality extends parallel to said axis, and

at least one layer at said near side and at most one layer less than said plurality of layers, wherein said at least one layer extends parallel to said axis.

39. The circuit in claim 38, wherein said near side is interposed between said far side and said first circuit device.

40. The circuit in claim 39, wherein said first circuit device is an electrically conductive device and said element is an electrically conductive element.

41. The circuit in claim 40, wherein said first circuit device is a conductive plug, said second circuit device is a capacitor, and said element is a capacitor electrode.

42. A fabrication method for an in-process substrate assembly including an insulator around a capacitor plate, wherein said insulator and said capacitor plate define a plane thereover, and said insulator includes a first portion contacting said plate and over-encompassing an opening site, said method comprising:

covering said first portion of said insulator with an oxide;

removing a part of said substrate assembly uncovered by said oxide, including

removing a second portion of said insulator contacting said capacitor plate and free of an opening site;

layering a dielectric over said plate and over said oxide;

layering a conductive material over said dielectric; and

planarizing said conductive material down to said oxide.

43. The method in claim 42, further comprising a step of etching an opening within said opening site.

44. The method in claim 43, wherein said step of layering a dielectric over said plate comprises layering a dielectric over a container-shaped plate.

45. The method in claim 44, wherein said step of layering a dielectric over a container-shaped plate comprises depositing said dielectric onto an interior of said container-shaped plate and a part of an exterior of said plate uncovered with said oxide.

46. The method in claim 45, wherein said step of removing a part of said substrate assembly comprises removing a flow-fill material from said interior of said container-shaped plate.

47. The method in claim 46, wherein said step of covering said first portion of said insulator with an oxide comprises:

layering said oxide onto said first portion of said insulator, said second portion of said insulator, and said plate; and

removing said oxide from said second portion of said insulator and said plate.

48. The method in claim 47, wherein said step of removing a part of said substrate assembly comprises:

plasma etching a portion of said substrate assembly; and

wet etching said portion of said substrate assembly.

49. A method of spacing a capacitor from a contact site, comprising:

providing insulation conformal to a first capacitor plate defining a container shape, wherein a first part of said insulation incorporates said contact site and a second part of said insulation is free of any contact site, and wherein said first plate and said insulation extend to a common height;

providing additional insulation in an interior of said container shape;

reducing a height of said first plate;

providing an etch mask over said first part of said insulation;

allowing said etch mask to extend over said interior;

removing said second part of said insulation and said additional insulation;

removing said etch mask;

depositing a capacitor insulator over said first plate and said first part of said insulation;

depositing a second plate over said capacitor insulator and over said first part of said insulation; and

removing said second plate from over said first part of said insulation.

50. The method in claim 49, wherein said step of removing said second plate comprises removing said second plate through chemical-mechanical planarization.

51. The method in claim 50, wherein said step of removing said second part of said insulation and said additional insulation comprises:

dry etching said second part of said insulation and at least some of said additional insulation; and

wet etching a remaining amount of said additional insulation.

52. A memory cell, comprising:

a bottom plate of a capacitor having an exterior vertical surface, wherein said surface defines a circumference; and

insulation incorporating a contact site and abutting said exterior vertical surface at a first region and separate from said exterior vertical surface at a second region.

53. The memory cell of claim 52, wherein said first region represents no more than 50% of said circumference.

54. The memory cell of claim 53 wherein said second region represents at least 50% of said circumference.

55. A method of spacing a contact site from a plurality of conductive elements, comprising:

providing an insulation layer enveloping said contact site;

etching an opening in said insulation layer, said opening being spaced from said contact site;

providing a first conductive element within said opening, said first conductive

element reaching an elevation lower than a top of said insulation layer;

protecting a first region of said insulation layer from etching, said first region including at least said contact site and an area extending from said contact site to said first conductive element

excluding a second region of said insulation layer from etch protection, said second region extending from said first conductive element and excluding any contact site;

etching said second region of said insulation layer;

providing a second conductive element over said first conductive element and over said first region of said insulation layer; and

removing a portion of said second conductive element over said first region of said insulation layer.

56. The method in claim 55, wherein said step of providing a first conductive element comprises:

providing a first conductive element reaching said top of said insulation layer; and

recessing said first conductive element.

57. The method in claim 56, wherein said step of providing a first conductive element comprises providing a conductive stud.

58. The method in claim 57, wherein said step of protecting a first region of said insulation layer comprises protecting a first region extending over said stud.

59. The method in claim 58 further comprising a step of providing a dielectric between said first conductive element and said second conductive element.

60. The method in claim 59, wherein:

said step of etching said second region of said insulation layer comprises etching a trench next to said first conductive element;

said step of providing a dielectric between said first conductive element and said second conductive element comprises lining said trench; and

said step of providing a second conductive element comprises filling said trench.

61. A method of providing double-sided capacitance and maintaining a distance between a capacitor and a contact site in a memory device, comprising:

encompassing said contact site within an insulation layer;

defining a container within said insulation layer, wherein said container is spaced from said contact site;

depositing a first conductive layer over said insulation layer, including depositing within said container and over said contact site;

removing a first part of said first conductive layer, wherein said first part is outside of said container;

recessing a second part of said first conductive layer, wherein said second part is inside of said container;

retaining a third part of said first conductive layer, wherein said third part is

outside of said container and over said contact site;

defining a recess in said insulation layer extending from said container and extending away from said contact site;

depositing a capacitor dielectric within said recess and over said second and third part of said first conductive layer;

depositing a second conductive layer over said capacitor dielectric; and

planarizing said second conductive layer, said capacitor dielectric, and said third part of said first conductive layer down to said insulation layer.

62. The method in claim 61, further comprising:

depositing photoresist over said first conductive layer;

patterning said photoresist before said removing and recessing steps;

guiding said removing and recessing steps with said photoresist; and

removing said photoresist before said step of depositing a capacitor dielectric.

63. The method in claim 62, wherein said step of patterning said photoresist comprises developing a portion of said photoresist over said contact site and over a portion of said insulation layer, said portion of said insulation layer extending from said contact site to said container, and wherein said portion of said photoresist is coextensive with said portion of said insulation layer.

64. The method in claim 63, further comprising allowing undeveloped photoresist to remain in said container during said removing and recessing steps.

65. The method in claim 62, wherein said step of patterning said photoresist comprises developing a portion of said photoresist over said contact site and over a portion of said insulation layer, said portion of said insulation layer extending from said contact site to said container, and wherein said portion of said photoresist extends beyond said portion of said insulation layer.

66. The method in claim 65, wherein said step of recessing a second part of said first conductive layer comprises:

anisotropically etching a first region of said second part uncovered by said photoresist; and

isotropically etching a second region of said second part covered by said photoresist.

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